WHAT IS CLAIMED IS:

1. An integrator circuit with a reset mechanism, comprising:

an integration capacitor;

a reset capacitor;

a first integration switch coupled between an input of said integrator and an input side of said integration capacitor;

a second integration switch coupled between an output side of said integration capacitor and an output of said integrator;

a third integration switch coupled between an input common mode voltage and an input side of said reset capacitor;

a fourth integration switch coupled between an output side of said reset capacitor and an output common mode voltage;

a first reset switch coupled between said input of said integrator and said input side of said reset capacitor;

a second reset switch coupled between said output side of said reset capacitor and said output of said integrator;

a third reset switch coupled between said input common mode voltage and said input side of said integration capacitor; and

a fourth reset switch coupled between said output side of said integration capacitor and said output common mode voltage, wherein said integration switches are closed during an integration mode and open during a reset mode, and wherein said reset switches are closed during said reset mode and open during said integration mode.

2. An integrator with a reset mechanism, comprising a replacement integration capacitor which replaces an integration capacitor during a reset mode of the integrator.

3. The integrator of Claim 2, wherein said integration capacitor is charged to a predefined voltage during said reset mode.

4. A method of resetting an integrator comprising temporarily removing an integration capacitor and replacing said integration capacitor with a reset capacitor during a reset operation of said integrator.

5. The method of Claim 4, further comprising charging said integration capacitor to a predefined voltage during said reset operation.

6. The method of Claim 4, wherein temporarily removing said integration capacitor and replacing said integration capacitor with said reset capacitor is repeated one or more times.

7. A delta-sigma modulator having a plurality of integration stages, wherein at least one of said integration stages comprises a first capacitor for integration and a second capacitor to replace the first capacitor in resetting said at least one integration stage.

8. A differential integrator, comprising a pair of normal integration capacitors and a pair of reset integration capacitors, wherein said normal integration capacitors are rotated out of the integrator and the reset integration capacitors are rotated into the integrator to reset the integrator.

9. A circuit for resetting a state variable output of an integrator, comprising:

a plurality of integration switches, wherein said integrator operates in a normal mode when said plurality of integration switches are closed;

a plurality of reset switches, wherein said plurality of reset switches are open when said plurality of integration switches are closed; and

at least one reset capacitor, wherein said reset capacitor replaces an integration capacitor between an input and an output of said integrator when said plurality of reset switches are closed and said plurality of integration switches are open.

10. A microphone, comprising a circuit for resetting a state variable output of at least one integrator, wherein said at least one integrator comprises a first capacitor for integration and a second capacitor to replace the first capacitor in resetting said at least one integrator.

11. A microphone, comprising:

a transducer;

a delta-sigma modulator, coupled to said transducer; and

means for maintaining said delta-sigma modulator in a stable state.

12. The microphone of Claim 11, wherein said means for maintaining said delta-sigma modulator in a stable state comprises a circuit for resetting a state variable output of an integrator of said delta-sigma modulator, comprising:

a plurality of integration switches, wherein said integrator operates in a normal mode when said plurality of integration switches are closed;

a plurality of reset switches, wherein said plurality of reset switches are open when said plurality of integration switches are closed; and

at least one reset capacitor, wherein said reset capacitor replaces an integration capacitor between an input and an output of said integrator when said plurality of reset switches are closed and said plurality of integration switches are open.

13. The microphone of Claim 12, wherein said means for maintaining said delta-sigma modulator in a stable state further comprises a limiter, coupled between said transducer and said delta-sigma modulator.